

Getting the Most Out of the New AT45DBxxxC DataFlash® Family

Introduction

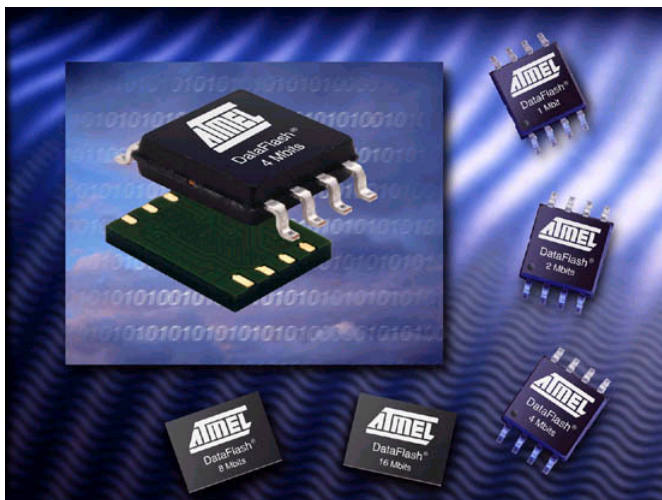
The AT45DB321C is the first member of a new family of low-cost, high-speed serial-interface DataFlash memories targeting a wide range of applications in the embedded and wireless markets. The AT45DB321C offers enhanced hardware and software features as well as smaller form factor packages optimized for a variety of digital voice, image, and program and data storage applications. The AT45DB321C also utilizes an intelligent adaptive algorithm during erase and programming operations for superior endurance over the product's lifetime.

Product Highlights

- Single 3V Read/Write Operation (2.7V - 3.6V Supply Range)
- SPI Mode 0 and Mode 3 Compatible
- Fast Read Access Times: 40 MHz Maximum Clock Frequency
- Individual Hardware and Software Sector Protection
- Security: 128-byte Register
- JEDEC Standard Manufacturer and Device ID Read
- Endurance: 100,000 Program/Erase Cycles per Page Minimum
- Data Retention: 20 Years
- New Small Form Factor Packaging Options: 8-pad CASON, 28-pin TSOP and 24-ball CBGA
- Green (Pb/Halide-free) Packaging Options

The AT45DB321C is offered in smaller form factor packages to dramatically reduce board real-estate. These new packages will provide an easy small footprint migration path to next generation, high-density DataFlash devices. The CASON and CBGA packages are ideal for wireless and portable applications where board space is critical. The CASON package is footprint compatible with the 8-pin SOIC and provides an easy density migration path in a compact 8-pin layout.

Figure 1. 8-pad CASON vs. 8-pin SOIC



Using the New DataFlash® AT45DBxxxC Family

Application Note (AN-9)



New Features and Benefits

Commands

The AT45DBxxx “C” family commands are fully backward compatible with the AT45DBxxx “B” family devices. In addition, the AT45DB321C device offers new functionality, which includes individual sector protection, security register and JEDEC ID.

For those customers using the legacy “inactive” modes, it is recommended to convert to the standard SPI commands. The legacy commands are supported in the “C” family to allow time for the system designers to make the necessary changes. These commands will not be supported in future products.

Manufacturer and Device ID Read

The AT45DB321C supports the JEDEC standard for manufacturer and device ID read. The manufacturer and device ID may be used during the boot-load process to identify the device and select the appropriate device drivers. This feature is useful where system designers need to provide a different opcode to multiple memory devices on the board.

Manufacturer and Device ID Command

Command	SCK Mode	Opcode
Manufacturer and Device ID Read	SPI Mode 0 or 3	9FH

Security Register

The “C” family devices contain a specialized register that can be used for security purposes in system design. The Security Register is a 128-byte one-time programmable (OTP) register that is divided into two sections. The first 64 bytes are user programmable, the remaining 64 bytes are factory programmed and will contain a number unique to every device. The register is separate from the main array and is read and programmed using different commands. Once the customer section of the register is programmed, it will be permanently locked to prevent reprogramming. This means that once this section is programmed, it can never be altered. The security register can be used to store manufacturer serial numbers and/or a small-encrypted security key for system authentication.

Security Commands

Command	SCK Mode	Opcode
Security Register Program	SPI Mode 0 or 3	9AH
Security Register Read	SPI Mode 0 or 3	77H

Individual Sector Protection

Protecting the contents of a flash memory device has always been an important consideration. The “C” family features flexible sector protection, so that critical contents can be kept secure while unprotected sectors are programmed and erased. Specifically, the AT45DB321C memory array is organized into 16 individual sectors that can be independently protected or unprotected.

The “C” family offers hardware and software controlled sector protection methods. The selection, of which sectors to be protected/unprotected from program and erase operations is defined by a specific register, called the Sector Protection Register. The software method uses a command sequence to enable sectors for protection specified by the sector protection register.

The hardware method utilizes the write protect (\overline{WP}) pin to protect sectors specified by the sector protection register. Once sector protection is enabled by either method, the contents of the selected sector are protected and cannot be erased or programmed. Software sector protection is useful in applications in which the write protect (WP) pin is

not or cannot be controlled by a host processor. The following command sequence is used to enable or disable Sector Protection:

Command	Byte 1	Byte 2	Byte 3	Byte 4
Enable Sector Protection	3DH	2AH	7FH	A9H
Disable Sector Protection	3DH	2AH	7FH	9AH

Please refer to the specific datasheet for more details.

Programming and Erase Operation

The “C” family of devices utilizes an intelligent adaptive algorithm for programming and erase operations. The adaptive algorithm is used to provide superior endurance while minimizing erase and programming time. To optimize system performance, Atmel recommends the user poll the status register RDY/BUSY bit or the RDY/BUSY pin instead of using fixed timing.

Design Considerations

1. The erase and programming operations are internally self-timed. Therefore, do not use fixed timing.
2. In order to minimize the erase and programming time, monitor the RDY/BUSY bit of the status register or the RDY/BUSY pin during erase or programming operation.

Conclusions

The AT45DB321C architecture and small form factor package options offer an easy density migration path for designers and manufacturers. In summary, the AT45DB321C DataFlash delivers:

1. Fast Read Access
2. Advanced Features
 - Security Register
 - Individual Sector Protection
 - JEDEC Standard Manufacturer and Device ID
3. High Endurance
4. Superior Data Retention
5. Small Form Factor Package Options

Comparison Between the AT45DBxxx “B” Family and the AT45DBxxx “C” Family

DC Characteristics

Symbol	Parameter	Condition	AT45DB321B			AT45DB321C			Units
			Min	Typ	Max	Min	Typ	Max	
V _{CC}	Supply Voltage		2.7		3.6	2.7		3.6	V
I _{SB}	Standby Current	\overline{CS} , \overline{RESET} , \overline{WP} = V _{CC} ; all inputs at CMOS levels		2	10		6	15	μA
I _{CC1}	Active Current Read Operation	f = 20 MHz; I _{OUT} = 0 mA; V _{CC} = 3.6V		4	10		10	15	mA
I _{CC2}	Active Current Program Operation	V _{CC} = 3.6V		15	35		35	50	mA
I _{CC3}	Active Current Erase Operation	V _{CC} = 3.6V		15	35		30	40	mA

AC Characteristics

Symbol	Parameter	AT45DB321B			AT45DB321C			Units
		Min	Typ	Max	Min	Typ	Max	
f _{SCK}	SCK Frequency			20			40	MHz
f _{CAR}	SCK Frequency for Continuous Read			20			40	MHz
t _{EP}	Page Erase and Programming Time			20		16	50	ms
t _P	Page Programming Time			14		8	14	ms
t _{PE}	Page Erase Time			8		8	40	ms
t _{BE}	Block Erase Time			12		20	250	ms

Packaging

Package Type	AT45DB321B	AT45DB321C	Comment
CASON	N/A	8-pad (6 x 8 x 1.0 mm)	Footprint compatible with 8-pin SOIC, 8-pin migration path
CBGA	44-ball (6 x 12 x 1.2 mm) 9-ball active matrix	24-ball (6 x 8 x 1.2 mm) 9-ball active matrix	Same active matrix, same ball pitch (1 mm) can fit into 44-ball footprints
TSOP	32-pin (8 x 20 x 1.2 mm)	28-pin (8 x 13.4 x 1.2 mm)	28 pin TSOP allows easy density migration path
SOIC	28-lead (0.330" wide body)	28-lead (0.330" wide body)	Not recommended for new designs. Future products will not support this package



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3519D-DFLSH-11/04